

What is claimed is:

[Claim 1] 1. A chip-packaging stack structure, comprising:

a plurality of chip-packaging units, suitable for stacking one over another, wherein each of the chip-packaging units comprises:
a substrate, having a top surface and a corresponding bottom surface, a plurality of upper contacts disposed on the top surface, and a plurality of lower contacts disposed on the bottom surface, wherein the upper contacts are electrically connected to the lower contacts respectively;
a chip disposed on the top surface of the substrate and having a plurality of inner contacts and a plurality of outer contacts, wherein the inner contacts are electrically connected to the outer contacts respectively;
a plurality of wires, respectively connected to the upper contacts and the inner contacts;
a molding compound covering the wires, the chip and the upper contacts of the substrate, wherein the molding compound has an opening for exposing the outer contacts; and
a plurality of solder balls, respectively connected to the lower contacts and being corresponding to the outer contacts of other chip-packaging units for electrically connecting the chip-packaging units.

[Claim 2] 2. The chip-packaging stack structure according to claim 1, wherein the outer contacts are disposed in central area on a surface of the chip, and the inner contacts are disposed in a periphery area on a surface of the chip.

[Claim 3] 3. The chip-packaging stack structure according to claim 2, wherein the outer contacts are disposed in a surface array distribution.

[Claim 4] 4. The chip-packaging stack structure according to claim 3, wherein the outer contacts are corresponding to the lower contacts, and the lower contacts are disposed in a surface array distribution in a central area of a surface of the bottom surface.

[Claim 5] 5. The chip-packaging stack structure according to claim 1, wherein the chip further comprises a plurality of bonding pads and a redistribution layer disposed on a surface of the chip, and the bonding pads are respectively connected through the redistribution layer to the inner contacts and the outer contacts.

[Claim 6] 6. The chip-packaging stack structure according to claim 1, wherein the chip further comprises a plurality of bonding pads, a portion of which constitute the inner contacts, and the other portion of which constitute the outer contacts.

[Claim 7] 7. The chip-packaging stack structure according to claim 1, wherein the chip-packaging units are disposed in a distribution of a ball grid array.

[Claim 8] 8. The chip-packaging stack structure according to claim 1, wherein the substrate is made of ceramic, glass, or plastics.

[Claim 9] 9. The chip-packaging stack structure according to claim 1, further comprising a heat dissipating plate, disposed on the top layer of the chip-packaging units and in the opening of the molding compound of the top layer.

[Claim 10] 10. A stacked structure for chip-packaging, comprising:
a first chip-packaging unit, having a substrate and a first chip, wherein the substrate has a top surface and a corresponding bottom surface, a plurality of upper contacts disposed on the top surface, a plurality of lower contacts disposed on the bottom surface and electrically connected to the upper contacts respectively, and wherein the first chip is disposed on the top surface and electrically connected to the upper contacts;
a second chip-packaging unit, having a carrier and a second chip disposed on the carrier, wherein the second chip has a plurality of inner contacts and a plurality of outer contacts, and the inner contacts are electrically connected to the carrier; and

a plurality of solder balls, respectively connected to the lower contacts and the outer contacts such that the first chip-packaging unit and the second chip-packaging unit are stacked and electrically connected.

[Claim 11] 11. The stacked structure for chip-packaging according to claim 10, wherein the outer contacts are disposed in a central area on a surface of the second chip, and the inner contacts are disposed in a periphery area on a surface of the second chip.

[Claim 12] 12. The stacked structure for chip-packaging according to claim 11, wherein the outer contacts are disposed in a surface array distribution.

[Claim 13] 13. The stacked structure for chip-packaging according to claim 12, wherein the outer contacts are corresponding to the lower contacts, and the lower contacts are disposed in a surface array distribution in a central area on the bottom surface.

[Claim 14] 14. A chip-packaging unit comprising:

a substrate, having a top surface and a corresponding bottom surface, a plurality of upper contacts disposed on the top surface, and a plurality of lower contacts disposed on the bottom surface, wherein the upper contacts are electrically connected to the lower contacts respectively;
a chip, disposed on the top surface of the substrate and having a plurality of inner contacts and a plurality of outer contacts;
a plurality of wires, respectively connected to the upper contacts and the inner contacts; and
a molding compound, covering the wires, the chip and the upper contacts of the substrate, and having an opening for exposing the outer contacts.

[Claim 15] 15. The chip-packaging unit according to claim 14, further comprising a plurality of solder balls disposed respectively on the lower contacts.

[Claim 16] 16. The chip-packaging unit according to claim 14, wherein the chip further comprises a plurality of bonding pads and a redistribution layer disposed on a surface of the chip, and the

bonding pads are respectively connected through the redistribution layer to the inner contacts and the outer contacts.

[Claim 17] 17. The chip-packaging unit according to claim 14, wherein the chip further comprises a plurality of bonding pads and a portion of the bonding pads constitute the inner contacts and the other portion of the bonding pads constitute the outer contacts.

[Claim 18] 18. The chip-packaging unit according to claim 14, wherein the substrate is made of ceramic, glass, or plastics.